Data Book
ZF SystemCard

Embedded System Card based on the *OEMmodule™*

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General Description

The ZF SystemCard is a full-featured embedded system computer utilizing the ZF MicroSystems OEMmodule. It is a complete PC/AT-compatible motherboard including standard peripheral interfaces. Its small size, low power consumption, and rugged construction makes it ideal for embedded systems. You can develop software directly on a SystemCard system or on a desktop PC/AT and transfer your code directly to an OEMmodule-based embedded system with little or no modification.

The SystemCard includes all standard motherboard functions, serial and parallel I/O, floppy and EIDE disk controllers, a high-performance CRT/flat-panel video controller, a 10BaseT Ethernet interface, an internal resident Flash disk for program storage, an optional True Flash File disk, programmable digital I/O port, PC/104 expansion bus, a standard PC/AT BIOS, and Embedded DOS™-ROM (EDOS-ROM).

For many systems, the standard PC ROM-BIOS and resident Flash disk with its EDOS-ROM eliminate the need for rotating media (such as a floppy or hard disk) for application program storage.

Industry Standard Compatibility

The SystemCard expansion bus conforms to the popular PC/104 standard. It allows you to easily integrate a wide variety of low-cost PC/104 peripherals in your embedded system. The SystemCard has a nonstack through PC104 connector.

The board's PC-compatible serial ports, parallel port, floppy interface, and hard disk interface allow you to use standard hardware, cables, and software libraries in your development program.

Features

100 MHz 486SX or 40 MHz 386SX CPU

- Full 32-bit internal architecture, cost-effective 16-bit external bus.
- Virtual memory, paging, and hardware-enforced protection.

PC Core Logic

- AT-compatible DMA controllers, interrupt controllers, timer/counters .
- AT keyboard controller.
- Real-time clock.

DRAM Controller

- High performance MUXed DRAM interleave, CPU pipelined operation.
- 2M DRAM in the OEMmodule.
- **486SX** only – 16M additional DRAM soldered on board.
- Supports up to 16M bytes additional DRAM in an SO-DIMM memory module (**386SX**).
- Shadowed BIOS for optimum performance.

Serial Ports

- Two 16550-type RS232C serial ports
- One 16450-type (386SX) or 16550-type (486SX) RS232C serial port and one 16450-type (386SX) or 16550-type (486SX) RS485 serial port.

Parallel Ports

- Two fully-compatible PC/AT parallel ports
- Supports bi-directional operation

Digital I/O

- 12 bits of TTL, input or output

Floppy Disk Controller

- Software compatible with 765B floppy controller and PC BIOS.
- Supports all standard PC floppy formats.

EIDE Hard Drive Interface

- Standard 40-pin interface to EIDE hard disk drive.
- Supports up to two EIDE drives (master/slave).

CRT/Flat-Panel Controller

- Based on Chips and Technologies 65545 Flat Panel/CRT GUI accelerator
- 512K byte video memory
- Fully compatible with VGA standard
- Hardware windows acceleration
- Supports non-interlaced CRT monitors with resolutions up to 1024 x 768 x 16 colors and 800 x 600 x 256 colors
- True-color and Hi-color display capability with flat panels and CRT monitors up to 640 x 480
- Direct interface to color and monochrome Dual Drive (DD) and Single Drive (SS) STN and TFT panels
- Supports 8, 9, 12, 15, 16, 18, and 24-bit data interfaces
- Supports power-sequencing controls for Vdd, Vee, and +12V to inverter for backlights
- Flat-Panel (3.3V and 5.0V) support with add-on daughter card (optional)

Ethernet Controller

- 10BaseT (twisted-pair), 10M bit/s
- Supports IEEE 802.3 (ANSI 8802-3) and Ethernet standards
- 386SX - Based on the Am79C961A PCnet™-ISA II full duplex Ethernet controller
- 4867SX – Based on the Realtek RTL8019AS full duplex Ethernet controller with Plug and Play function
- Supports AUI to external 10Base2, 10Base5, 10BaseT or 10BaseF MAU.
- Supports full duplex operation on the 10BaseT and AUI ports
- LNKST and RCV LEDs for line verification
- Boot PROM capability for booting from network
- Supports Microsoft's Plug and Play System configuration
- Broad NOS support, including Novell Netware, Microsoft Windows 95, Microsoft LAN Manager, SCO UnixWare, IBM LAN Server, SunSoft PC-NFS, SunSoft Solaris, Artisoft LANtastic, Banyan Vines

Solid-State Flash Storage

- 1.4M byte (**486SX**) or 180K byte (**386SX**) Flash EPROM, available for OS and OEM software
- DOS-compatible BIOS in Flash EPROM
- Solid-State CompactFlash
- Support for CompactFlash removable cartridge
- 2M to 60M bytes or more storage
- Can be configured to be the boot drive

Configurable Memory Sockets

- **386SX** – Two 32-pin byte-wide memory sockets.
- **486SX** - One 32-pin byte-wide memory socket
- Supports popular 5V JEDEC Flash EPROMs and Non-volatile NVRAM devices
- Configurable addressing

Embedded DOS-ROM

- Similar to the popular DOS operating systems, but specifically designed for embedded systems
- Supports standard desktop software, including Windows 3.1, Windows 95, Norton Utilities
- DOS-like command-line interface
- Option: Embedded DOS 6-XL, a fully multi-threaded DOS-like OS

PC BIOS

- Standard PC BIOS functionality.
- Easy to upgrade using ZF MicroSystem's unique Download Interface.
- Setup information is stored in non-volatile Flash EPROM. Allows battery-free operation.

Embedded Disk Operating System

- Supports most PC/AT-compatible operating systems, including MS-DOS
- Support for standard desktop software, including Windows 3.1, Windows 95, Norton Utilities
- Supports Embedded DOS 6-XL, fully multi-threaded version of the standard PC DOS

Expansion Bus

- Supports the PC/104 expansion bus (nonstack through version)
- Add up to three PC/104 modules

Power Monitor

- Brownout protection, provides reliable reset signal if power fluctuates.
- Resistor-configurable voltage threshold.

Electrical Specifications

- 386SX - Requires +5VDC @ 1 amp ±5% (2 MB internal DRAM).
- 486SX – Requires +5VDC @ 1.2 amps ±5% (18MB DRAM)
- Future support for low-power modes.

Mechanical Specifications

- 5.75” x 8.00” (146mm x 203mm)
- PC/104 bus compliant with PC/104 V2 specification.
- Standard ribbon cable connectors for floppy, EIDE, serial, and parallel interfaces.

Environmental Specifications

- Operating temperature: 32F to 158F (0C to 70C).
- Storage temperature: -67F to 185F (-55C to 85C).
- Weight: 10.5 oz (300 gm).

ORDERING INFORMATION

SCX-486-Q-02/SCX-386-Q-02 — ZF SystemCard. SystemCard form factor, includes OEMmodule, with 18M byte DRAM, built-in Flash, SVGA controller, 10BaseT Ethernet controller, Compact Flash interface, speaker, BIOS and Embedded DOS-ROM.

SCX-486-K-02/SCX-386-K-02 — ZF SystemCard Development Kit. SystemCard form factor, includes OEMmodule, with 18M byte DRAM, built-in Flash, SVGA controller, 10BaseT Ethernet controller, Compact Flash interface, speaker, BIOS and Embedded DOS-ROM, technical manuals, cables, and utility software. Does not include external DRAM.

Contents

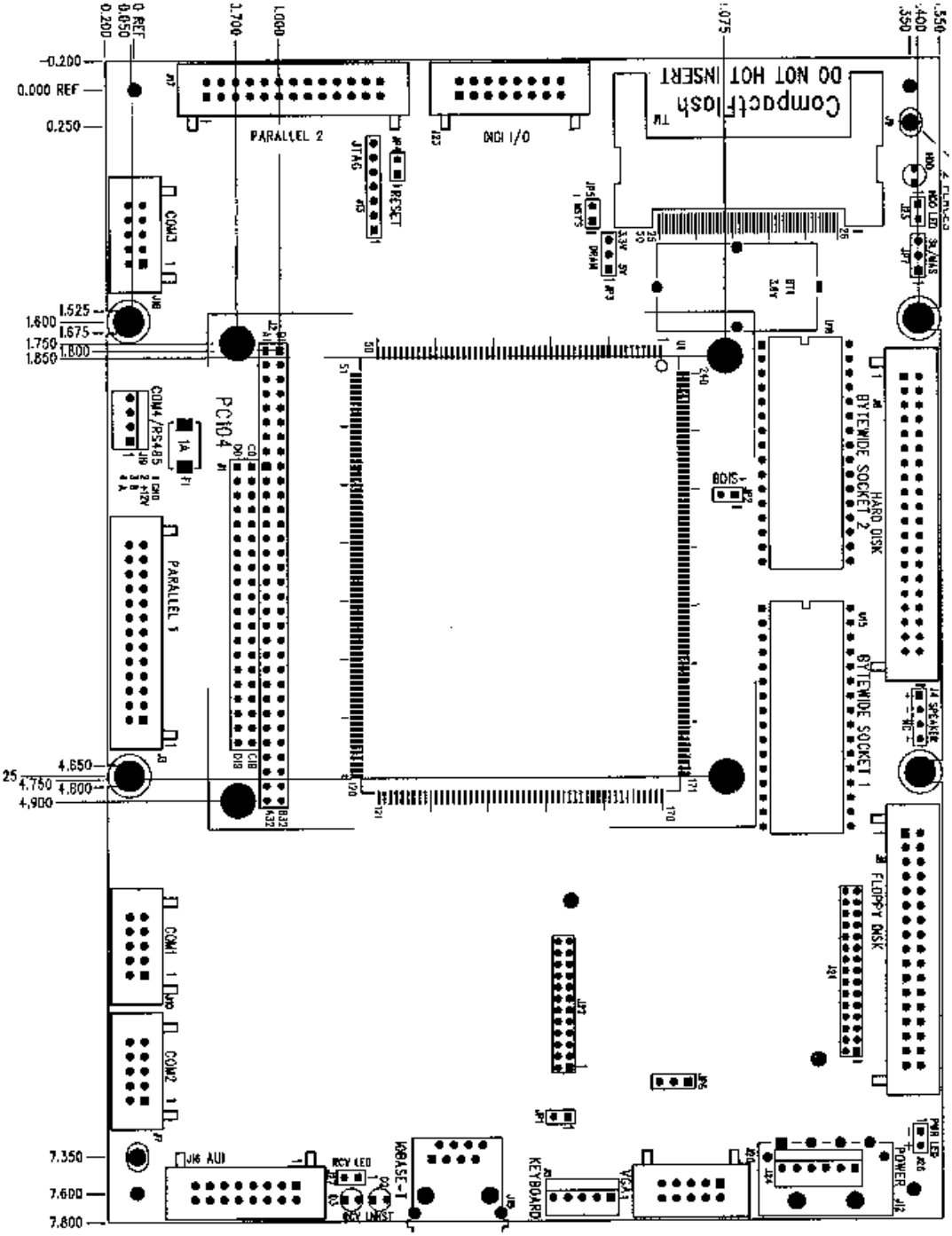

Figure 1. Board Dimensions

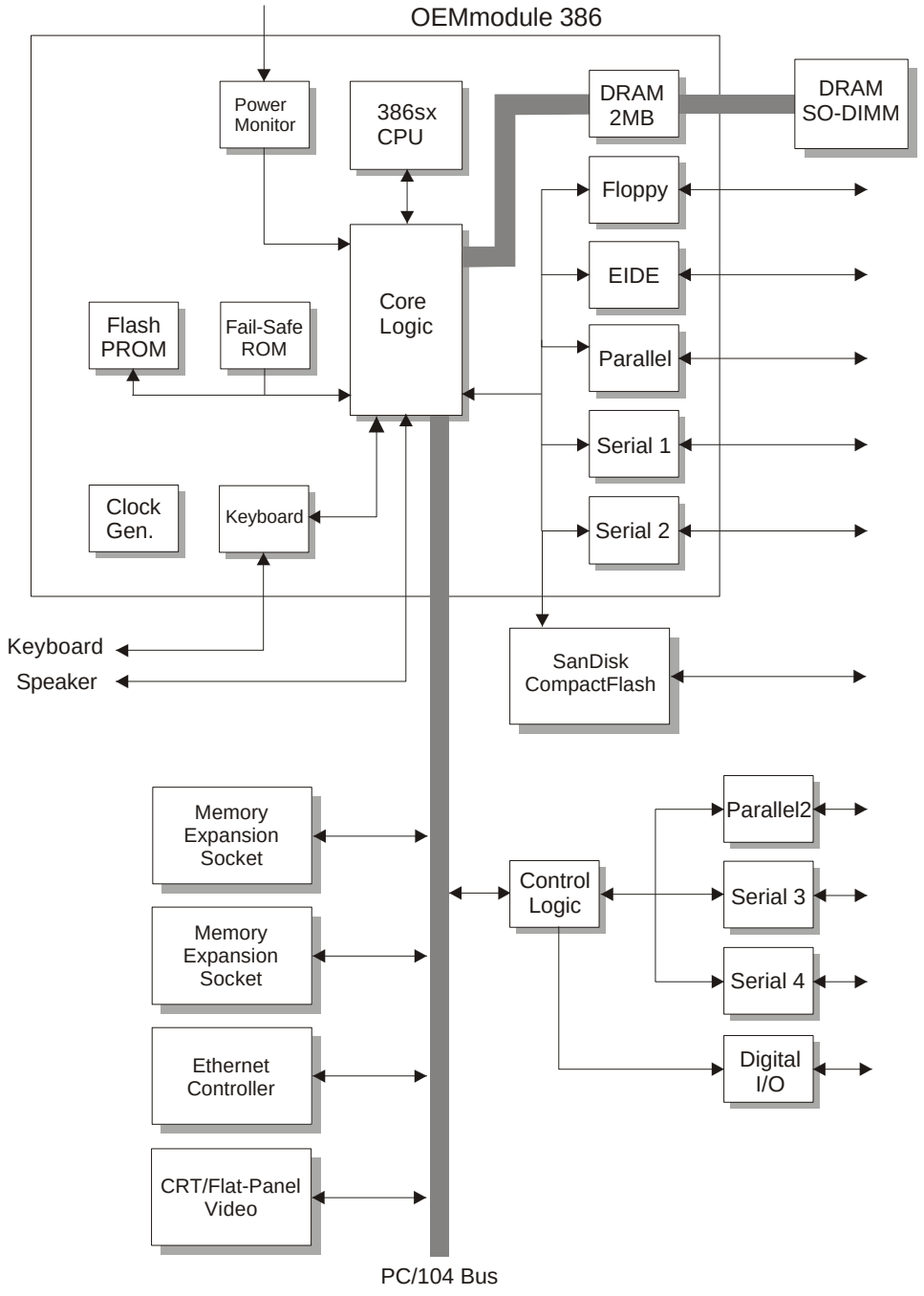

Figure 2. System Block Diagram

Connector Summary

Most connections to the SystemCard are made through I/O connectors J3 through J27 and the PC/104 bus connectors J1 and J2. Table 1 summarizes the use of J1 through J12.

Connector	Function	Type
J1	PC/104 C/D	40-Pin Dual Row, .100 centers
J2	PC/104 A/B	64-Pin Dual Row, .100 centers
J3	Parallel 1	26-Pin Dual Row, .100 centers
J4	Speaker	4-Pin, Single Row, .100 centers
J5	Keyboard	5-Pin, Single Row, .100 centers
J6	Floppy	34-Pin Dual Row, .100 centers
J7	Serial 2	10-Pin Dual Row, .100 centers
J8	EIDE	40-Pin Dual Row, .100 centers
J9	CompactFlash Socket	50-Pin, SanDisk Standard
J10	Serial 1	10-Pin Dual Row, .100 centers
J11	SO-DIMM Socket	72-Pin (386SX only)
J12	Power (standard)	4-Pin, Standard PC Power
J13	JTAG	6-Pin Single Row, .100 centers
J15	10BaseT Ethernet	RJ45
J16	AUI Ethernet	16-Pin Dual Row, .100 centers
J17	Parallel 2	26-Pin Dual Row, .100 centers
J18	Serial 3	10-Pin Dual Row, .100 centers
J19	Serial 4 (RS485)	4-Pin, Single Row, .100 centers
J20	VGA	10-Pin, Dual Row, .100 centers
J21	Flat Panel I/F 2	30-Pin
J22	Flat Panel I/F 1	24-Pin
J23	Digital I/O	16-Pin
J24	Alternate Power (factory option)	6-Pin Single Row, .100 centers
J25	HDD Access LED	2-Pin
J26	Power LED	2-Pin
J27	Ethernet RCV LED	2-Pin

Table 1. Connector Summary

Jumper Summary

The SystemCard provides a number of jumper options to configure features on the board. The jumpers, labeled “JP*n*”, are configured with 2mm shorting blocks. Table 1 shows a summary of the jumpers, their functions, and the factory default settings. For jumper options with more than two pins, default shorted pin-pairs are listed as *n1*/*n2*.

Jumper	Function	Default
JP1	Keyboard Lock	Off
JP2	Internal BIOS Enable (BDIS-) On=Fail-Safe ROM, Off=Flash BIOS	Off
JP3	**386SX only** - DRAM voltage1/2=5V, 2/3=3.3V	1/2
JP4	Reset (external reset connection; a ground on pin 1 resets the system)	Off
JP5	CompactFlash Type On=M-Systems	Off
JP6	Flat-Panel Signal Levels 1/2=5V, 2/3=3.3V	1-2
JP7	Compact Flash Master/Slave 1/2=Master, 2/3=Slave	Off

Table 2. Jumper Summary

DRAM Interface

The SystemCard is supplied with 2M bytes of DRAM which is internal to the OEMmodule. On the **386SX**, you can add up to 16M bytes in the form of an SO-DIMM module. The **386SX** has an SO-DIMM connector, mounted on the bottom of the board, for standard 72-pin SO-DIMM modules. Any standard page-mode SO-DIMMs *non-doubled sided* memory modules, with 70nS (or better) access time, can be used. The interface is designed to support fast page-mode DRAMs. EDO DRAMs are currently not supported. The **486SX** has 16M bytes of DRAM which is soldered on the board and an option for up to 16M bytes of additional DRAM soldered on board.

DRAM Voltage Option

Both 3.3 Volt and 5 Volt SO-DIMM modules are supported.

- For 3.3V SO-DIMM operation, on the **486SX**: install a 0 ohm resistor at R57.

  On the **386SX**: install a jumper block on JP3 1/2.

- For 5V operation, on the **486SX**: install a 0 ohm resistor at R58.

  On the **386SX**: install a jumper block on JP3 2/3.

Setting Memory Size

The BIOS automatically senses the amount of memory installed in your system and displays that information on the Setup configuration page. There is no user setting.

Power and Utility Connector

+5 Volt and +12 Volt power are supplied through the 4-pin connector, J12. The SystemCard also has an alternate 6 pin power connector, J24, which also supplies –5 and –12 volts. Contact your ZF MicroSystems sales representative for details.

+5 Volts is used for the board's main logic supply. The pinout of this connector matches the pinout found on standard floppy disk drives, hard disks, and so forth. Standard PC power supplies can be used without special cables.

Connect +12V to provide fused +12V to the RS485 serial interface (J19-2) and to the Ethernet AUI interface (J16-10). A 1 Amp resettable fuse, F1, is provided on the board for this purpose. +12V may also be required if you connect a flat-panel display to a flat-panel daughter card mounted on J21 and J22.

Table 3 lists the power pins on J12. Table 4 lists the power pins on J24.

Pin	Description
1	+12 Volts
2	Ground
3	Ground
4	+5 Volts

Table 3. Power Connector, J12

Pin	Description
1	-12 Volts
2	-5 Volts
3	+5 Volts
4	Ground
5	Ground
6	+12 Volts

Table 4. Alternate Power Connector, J24

The J24 connector is from AMP, part number 641215-6 and a typical mating connector is AMP, part number 641237-6.

KEYBOARD

The SystemCard provides the standard keyboard signals on connector J5. Table 5 shows how to wire a DIN-5 connector for a standard PS/2 keyboard cable.

Signal Name	Pin	Function	5-Pin DIN
N/C	1	N/C	
KBClock	2	Keyboard Clock	1
Power	3	+5 Volts	5
KBData	4	Keyboard Data	2
Ground	5	Ground return	4

Table 5. Keyboard Connector, J5

SPEAKER

Small piezoelectric speakers or standard PC speakers (with an 8 ohm coil) can be directly driven by the SystemCard through connector J4. The port supplies approximately 0.1 watt to the speaker. The speaker signal is TTL, current-limited with a series 33 ohm resistor. High frequencies are rolled off with a 0.01 µF capacitor (to ground).

Table 6 shows the pinout of J4.

Signal Name	Pin	Description
Speaker +	1	+5 Volts
Speaker -	2	Signal
GND	3	Ground
Speaker -	4	Signal

Table 6. Speaker Connector, J4

REAL-TIME CLOCK BATTERY

The real-time clock requires a 3.6 volt lithium cell to maintain the correct time, date, and CMOS memory values when power is off. An 850 mAh lithium cell is supplied with the board, providing up to 10 years of power for the real-time clock and CMOS memory.

If the battery fails and +5 Volt power is removed, the RTC will lose the current time and date, but the Setup data will remain intact. CMOS configuration information is always read from a Flash EPROM copy (inside the OEMmodule) if there is a fault detected in the contents of the Setup parameters stored in the CMOS RAM portion of the RTC.

Serial Ports

The SystemCard provides three full-featured PC-compatible asynchronous RS232C serial ports and one RS485 serial port. The serial ports are treated as COM1, COM2, COM3 and COM4 devices by DOS.

Standard system resources are allocated to the serial ports, as shown in Table 7:

Serial Port	Connector	Typical Usage	I/O Address	Standard Interrupt
Serial 1	J10	COM1	3F8h–3FFh	IRQ4 (shared)
Serial 2	J7	COM2	2F8h–2FFh	IRQ3 (shared)
Serial 3	J18	COM3	3E8h–3EFh	**386SX** – IRQ3 **486SX** – Programmable
Serial 4	J19	COM4	2E8h–2EFh	**386SX** – IRQ4 **486SX** - Programmable

Table 7. Serial Port Resources

RS232 SERIAL PORT CONNECTORS

The RS232 serial ports (Serial 1, Serial 2, and Serial 3) are brought out to 10-pin dual-row ribbon-cable connectors J10, J7, and J18. The connector pins are arranged to make it easy to construct a simple straight-through ribbon cable to a panel-mount DB-9 connector.

A full complement of input and output handshaking lines are implemented. Signals are at standard RS232C levels. Power for the RS232 voltage levels (-9V > x > +9V) is converted on-board from the +5V supply.

Pinouts for the serial connectors and for standard DB-9 connectors are shown in Table 4.

J10, J7 J18	DB-9 Pin	Signal	Function	In/Out
1	1	DCD	Data Carrier Detect	Input
3	2	RXD	Receive Data	Input
5	3	TXD	Transmit Data	Output
7	4	DTR	Data Terminal Ready	Output
9	5	GND	Signal Ground	
2	6	DSR	Data Set Ready	Input
4	7	RTS	Request To Send	Output
6	8	CTS	Clear To Send	Input
8	9	RI	Ring Indicator	Input
10		N/C	Ground	

Table 8. Serial Port Connectors, J10, J7, J18

386SX

Serial1, Serial2, and Serial3 are always enabled and require no setup. Serial1 and Serial3 are connected to IRQ4. Serial2 is connected to IRQ3.

486SX

Serial 1 is always enabled and requires no set up.

Serial 2 and Serial 3 can be ENABLED/DISABLED in the Custom Setup Screen in the CMOS setup. Options for Serial2 and Serial3 interrupts can be selected in the Custom Setup Screen. Options for Serial2 are IRQ3, IRQ4, or DISABLED and options for Serial3 are IRQ4, IRQ5, or DISABLED.

RS485 SERIAL PORT CONNECTOR, J19

Serial 4 is an RS485 serial port based on a 16450-equivalent UART. You can use the RS485 port as a low cost, easy-to-use communications and networking multi-drop interface. It can be used in a wide variety of embedded applications requiring low-to-medium-speed data transfer between two or more systems.

The following are some examples of interconnection schemes that can be used to take advantage of the RS485 port:

- **One-way Broadcast** — A single device, set in transmit mode, uses an RS485 signal pair to transmit data to many receiving devices.
- **Simple Bi-Directional Communication** — Two devices use a single RS485 bi-directional pair for half-duplex, two-way transmission of data. Only one device is permitted to talk at any one time. A port is placed in transmit mode under control of the network software, either by a simple alternation scheme or by messages contained within data packets.
- **Multi-Drop Network** — More than two devices share an RS485 signal pair, for both transmission and reception of data. Only one device is permitted to talk at any one time. All RS485 transceivers are placed in receive mode except the one permitted to transmit. One popular protocol for managing who is the transmitter is by a “token” passing scheme. Each node is assigned an ID number. Whichever node transmits also sends the ID of the next node allowed to transmit. If a node does not need to transmit, it immediately sends the “token” indicating who can talk next. Time-outs can be implemented in software to prevent a lockup should a node fail to pass the token properly.

The RS485 serial port is brought out to a 4-pin single row connector. Table 9 lists the pinout of this connector.

Signal Name	Pin	Description
Ground	1	Ground
+12V Fused	2	+12V Fused
B	3	Signal B (-)
A	4	Signal A (+)

Table 9. RS485 Connector, J19

The RS485 interface specification requires that both ends of the twisted-pair cable be terminated with 100 ohm resistors.

386SX

Serial4 is always enabled and is connected to IRQ3. The RS485 driver and receiver are controlled by RTS.

486SX

You can configure the Serial4 interface using the Custom Setup Screen in the CMOS Setup. The CMOS Setup allows you to enable or disable the port, select its IRQ (IRQ3, IRQ5, DISABLED), and select how you want to control the RS485 driver and receiver.

SERIAL PORT INTERRUPT SHARING

The COM1 and COM2 serial port interrupt request lines comply with the interrupt sharing scheme described in the PC/104 Version 2.3 specification. For a copy of the PC/104 Version 2.3 specification, visit the PC/104 Consortium web site (www.controlled.com/pc104). This sharing scheme is described in the OEMmodule Data Book.

The interrupt request lines from Serial 1 and Serial 2 are internally buffered in the OEMmodule with open collector buffers and internally connected to inputs IRQ4 and IRQ3 respectively. Internal 1000 ohm termination resistors hold the interrupt signals at logic 0 until an interrupt occurs. Other interrupt sources can be wire-ORed with either of these IRQ lines as long as they also follow the PC/104 interrupt sharing convention. The interrupt request signals appear on the PC/104 bus.

Note: The 1000 ohm pull-down resistor for each interrupt is provided on the board. Do not attach an external pull-down resistor.

Parallel Ports

The SystemCard parallel ports are fully compatible with the PC/AT parallel port. In the extended mode, they function as PS/2-like bi-directional ports.

The parallel ports use the following PC resources (Table 10):

Parallel Port	Connector	Typical Usage	I/O Address	Standard Interrupt
Parallel 1	J3	LPT1	3BCh – 3BFh (386SX) 378h – 37Fh (486SX)	IRQ7
Parallel 2	J17	LPT2	278h – 27Fh	IRQ5

Table 10. Parallel Port Resources

PARALLEL PORT SIGNALS

The parallel port output signals provide up to 48 mA drive current (active low). .0022 μF capacitors are connected from each data line to ground for noise suppression.

PARALLEL PORT REGISTERS

Table 11 summarizes the parallel port register interface. In this table, “A” indicates the port’s base address, for example, 3BCh.

Register	Bit	Signal Name	In/Out	Active High/Low
Data (A+0)	0	PD0	I/O	High
	1	PD1	I/O	High
	2	PD2	I/O	High
	3	PD3	I/O	High
	4	PD4	I/O	High
	5	PD5	I/O	High
	6	PD6	I/O	High
	7	PD7	I/O	High
Status (A+1))	0	1	-	-
	1	1	-	-
	2	1	-	-
	3	ERR-	In	Low
	4	SLCT-	In	High
	5	PE	In	High
	6	ACK-	In	High
	7	BUSY	In	Low
Control (A+2)	0	STRB-	Out	Low
	1	AUTOFD-	Out	Low
	2	INIT-	Out	High
	3	SLIN-	Out	Low
	4	IRQ ENABLE	-	High
	5	1	-	-
	6	1	-	-
	7		-	-

Table 11. Parallel Port Registers

The parallel port signals appear on J3 and J17, 26-pin dual-row ribbon-cable connectors. The ports may be cabled to appear on standard PC DB-25 connectors.

Table 12 shows the parallel port signals that appear on J3 and J17 and the equivalent pinout on DB-25S connectors.

J3 J17	DB-25S Pin	Signal	Function	In/Out
1	1	STRB-	Output Data Strobe	Output
2	14	AUTOFD-	Auto Feed	Output
3	2	PD0	Data Bit 0	I/O
4	15	ERR-	Printer Error	Input
5	3	PD1	Data Bit 1	I/O
6	16	INIT-	Initialize Printer	Output
7	4	PD2	Data Bit 2	I/O
8	17	SLIN-	Selects Printer	Output
9	5	PD3	Data Bit 3	I/O
10	18	GND	Signal Ground	N/A
11	6	PD4	Data Bit 4	I/O
12	19	GND	Signal Ground	N/A
13	7	PD5	Data Bit 5	I/O
14	20	GND	Signal Ground	N/A
15	8	PD6	Data Bit 6	I/O
16	21	GND	Signal Ground	N/A
17	9	PD7	Data Bit 7	I/O
18	22	GND	Signal Ground	N/A
19	10	ACK-	Character Acknowledged	Input
20	23	GND	Signal Ground	N/A
21	11	BUSY	Printer Busy	Input
22	24	GND	Signal Ground	N/A
23	12	PE	Out Of Paper	Input
24	25	GND	Signal Ground	N/A
25	13	SLCT	Printer Selected	Input
26	N/A	GND	Signal Ground	N/A

Table 12. Parallel Port Connectors, J3 and J17

PARALLEL PORT CONFIGURATION

386SX

The first parallel port, LPT1, is always enabled and appears at address 3BCh. It is connected, by default, to IQ7. The interrupt can be disabled by writing to the port's control register (Control port, bit 4. See Table 11). LPT2 is always enabled with no interrupt connection. LPT2 is always configured as standard output-only.

486SX

The first parallel port, LPT1, appears at address 378h. It is connected, by default, to IRQ7. The interrupt can be disabled in the Custom Setup Screen in CMOS Setup. . The port can be configured as output-only, bi-directional, EPP, DISABLED by choosing one of options in the Custom Setup Screen in CMOS Setup.

You can configure LPT2 using the Custom Setup Screen in CMOS Setup. It allows you to enable or disable the port and enable its IRQ (IRQ5).

Floppy Interface

A DOS-compatible floppy drive interface is supplied on J6. This interface allows cable connection to two floppy drives. In PC-compatible systems, the BIOS and DOS support these drives as A: and B:. These are configured using the BIOS Setup function.

Table 13 shows the PC resources used by the floppy subsystem.

Resource	Function
I/O Address 3F0h-3F7h	3F2 FDC Digital Output Register (LDOR) 3F4 FDC Main Status Register 3F5 FDC Data Register 3F7 FDC Control Register (LDCR)
IRQ6	Interrupt
DRQ2–DACK2	DMA Controller Channel

Table 13. Floppy Interface Resources

The floppy drive interface supports the standard PC floppy disk formats, 360K, 1.2M, 720K, and 1.44M. You must specify the type of drives connected to the floppy interface in the BIOS CMOS Setup. Press <Del> during the Power-On Self Test (POST) to enter Setup. The first drive typically appears to DOS as drive A:, and the second drive as B:.

Floppy drives are normally connected to a system using ribbon cables. The typical PC connection for dual floppy drives uses a special cable with certain ribbon cable wires (conductors 10 through 16) reversed between the two floppy connectors. Using this arrangement, all floppy drives can be jumpered for drive select 1 (the "second" drive). The wires to drive B: are unswapped.

Note: The board's internal Resident Flash Disk, if enabled, will be drive A and any floppy disk drive configured as drive A will become Drive B automatically. Only two floppy drives (A and B) are supported.

Table 14 lists the signals on the J6 floppy interface.

J6 Pin	Signal Name	Function	In/Out
2	DENSEL	Speed/Precomp	
4	N/A		N/A
6	N/S	Key Pin	N/A
8	INDEX-	Index Pulse	In
10	MTR0-	Motor On 0	Out
12	DRV1-	Drive Select 2	Out
14	DRV0-	Drive Select 1	Out
16	MTR1-	Motor On 1	Out
18	DIR-	Direction Select	Out
20	STEP-	Step Pulse	Out
22	WDATA-	Write Data	Out
24	WGATE-	Write Gate	Out
26	TRK0-	Track 0	Input
28	WRPRT-	Write Protect	Input
30	RDATA-	Read Data	Input
32	HDSEL-	Head Select	Out
34	DSKCHG-	Disk Change	Input
1– 33 (Odd)	Ground	Ground	

Table 14. Floppy Drive Connector, J6

EIDE Interface

The SystemCard is supplied with a standard EIDE Hard Disk Interface at connector J8. This is the standard interface used in PC-compatible systems for hard disk drives, CD-ROM drives, and certain other peripherals.

Up to two drives can be connected in a master-slave arrangement. Generally, the first hard disk drive (master drive) will appear as the C drive to DOS. The second drive (slave drive), if attached, will appear as drive D.

If you use the SanDisk CompactFlash, it is installed as an IDE drive in the system. Like an actual IDE drive, you can jumper the SanDisk to be a master or slave. Configure your IDE drive appropriately.

Table 15 lists the resources used by the EIDE interface.

Resource	Function
I/O Address 1F0h-1F7h	Hard Disk Interface
IRQ14	Interrupt

Table 15. EIDE Interface Resources

Use Setup to enable your attached hard drives. You must match the drive parameters in Setup with the actual parameters of your connected drive(s).

EIDE drives are typically attached to the drive interface with a 40-pin ribbon cable. Miniature drives sometimes require a cable adapter circuit board for translation between the standard 0.1 inch-spacing connector and the smaller connector on the drive. These generally are supplied with the drive.

The pinout for the EIDE interface, J8, is shown in Table 16.

Note: Due to drive manufacturer's different implementations of the master/slave arrangement, it may not be possible to properly configure two IDE drives from different sources to share the EIDE bus.

J8 Pin	Signal Name	Function	In Out	J8 Pin	Signal Name	Function	In Out
1	HDRESET-	Reset signal from host	OUT	21	N/A	Reserved	N/C
2	GND	Ground		22	GND	Ground	
3	HDD07	Data bit 7	I/O	23	HDIOW-	Write strobe	OUT
4	HDD08	Data bit 8	I/O	24	GND	Ground	
5	HDD06	Data bit 6	I/O	25	HDIOR-	Read strobe	OUT
6	HDD09	Data bit 9	I/O	26	GND	Ground	
7	HDD05	Data bit 5	I/O	27	RSVD	Reserved	N/C
8	HDD10	Data bit 10	I/O	28	HDALE	Address latch enable	OUT
9	HDD04	Data bit 4	I/O	29	RSVD	Reserved	N/C
10	HDD11	Data bit 11	I/O	30	GND	Ground	
11	HDD03	Data bit 3	I/O	31	IRQ14	Drive interrupt request	IN
12	HDD12	Data bit 12	I/O	32	IOCS16-	I/O Chip Select 16	In
13	HDD02	Data bit 2	I/O	33	HDA1	IDE Address 1	Out
14	HDD13	Data bit 13	I/O	34	RSVD	Reserved	N/C
15	HDD01	Data bit 1	I/O	35	HDA0	IDE Address 1	Out
16	HDD14	Data bit 14	I/O	36	HDA2	IDE Address 2	Out
17	HDD00	Data bit 0	I/O	37	HDCS0-	IDE Chip Select 0	Out
18	HDD15	Data bit 15	I/O	38	HDCS1-	IDE Chip Select 1	Out
19	GND	Ground		39	LEDIN-		
20	KEY	Keyed pin	N/C	40	GND	Ground	

Table 16. EIDE Drive Connector, J8

SVGA CRT/Flat-Panel Video Controller

The SystemCard provides a CRT/Flat-Panel video controller, based on the Chips and Technology 65545 Flat-Panel VGA controller. It is hardware-level register compatible with existing PC video standards. It supports CRT-only and flat panel-only display modes.

The controller is equipped with 512K bytes or 1M bytes of video memory (factory option), which supports standard VGA resolutions and SVGA resolutions up to 800 x 600 in 256 colors and up to 1024 x 768 in 16 colors, interlaced or non-interlaced (CRT).

The controller includes a PC-compatible video BIOS stored in Flash EPROM. The Flash EPROM can easily be reprogrammed with BIOSes customized for a wide variety of flat-panel displays.

CRT INTERFACE

The CRT video signals are brought out to J20, a 10-pin dual-row ribbon cable connector. Most PC-compatible multi-frequency monitors require a DE15 connector. Pinouts for J20 and a DE15 connector are shown in Table 17.

J20	Signal	DE15 Pin
1	Red	1
3	Green	2
5	Blue	3
7	Horizontal Sync	13
9	Vertical Sync	14
2, 4, 6, 8, 10	Ground	5, 6, 7, 8, 10
	No Connection	4, 9, 11, 12, 15

Table 17. CRT Connector, J20

FLAT-PANEL INTERFACE

Signals for a wide range of flat-panel displays, both color and gray scale, appear on connectors J21 and J22. These connectors are designed to interface to a “daughter card,” which in turn interfaces to a particular panel or family of panels. A daughter card provides for any additional circuitry that may be needed, such as contrast control logic, backlight power connections, Vee power supply converters, power sequencing and management circuits, and for the panel’s specialized ribbon-cable connectors.

Table 18 and Table 19 list the signals on J21 and J22 respectively. A full set of flat-panel signals are provided. Note that current flat panels do not share a standardized connector pin configuration. Even the names of panel control signals vary from manufacturer to manufacturer. Review the manufacturer’s documentation to ascertain what signals are required to drive the flat panel you choose.

Pin	Signal Name	Description	Pin	Signal Name	Description
1	P4	Data 4	2	P5	Data 5
3	Gnd	Ground	4	P6	Data 6
5	P7	Data 7	6	Gnd	Ground
7	P8	Data 8	8	P9	Data 9
9	Gnd	Ground	10	P10	Data 10
11	P11	Data 11	12	Gnd	Ground
13	P12	Data 12	14	P13	Data 13
15	Gnd	Ground	16	P14	Data 14
17	P15	Data 15	18	Gnd	Ground
19	P16	Data 16	20	P17	Data 17
21	Gnd	Ground	22	P18	Data 18
23	P19	Data 19	24	Gnd	Ground
25	P20	Data 20	26	P21	Data 21
27	Gnd	Ground	28	P22	Data 22
29	P23	Data 23	30	Gnd	Ground

Table 18. Flat-Panel Interface Connector, J21

Pin	Signal Name	Description	Pin	Signal Name	Description
1	+12 V	+12 V Power	2	+12 V	+12 V Power
3	DA CS	Serial EEPROM Chip Select 1*	4	ENABKL	Enable backlight power
5	ENAVEE	Enable Vee. Power sequencing control	6	+5 V	+5 V Power
7	FLM	First Line Marker. Flat panel equivalent of VSYNC	8	ENAVDD	Enable Vdd. Power sequencing control
9	LP	Latch Pulse. Flat panel equivalent of HSYNC.	10	+5 V	+5 V Power
11	M	Sometimes called AC Drive, BLANK, or Display Enable (DE).	12	Gnd	Ground
13	SHFCLK	Shift Clock. Pixel clock for flat panel data	14	Gnd	Ground
15	P0	Data 0	16	P1	Data 1
17	Gnd	Ground	18	P2	Data 2
19	P3	Data 3	20	Gnd	Ground
21	EE DO	Serial EEPROM Data Out*	22	EE DI	Serial EEPROM Data In*
23	EE SK	Serial EEPROM Clock*	24	EE CS	Serial EEPROM Chip Select 2*

Table 19. Flat-Panel Interface Connector, J22

* These signals are used to read and write EEPROMs on some flat-panel daughter cards.

FLAT-PANEL DISPLAY VOLTAGE

Current flat panels use either +5 volts or 3.3 volts. The flat-panel daughter card has an on-board voltage regulator to provide 3.3 volt control signals to a flat panel. Use jumper J6 on the SystemCard to select between +5V and +3.3V signals. Install a jumper on JP6-1/2 to select +5 Volts or JP6-2/3 to select +3.3 Volts.

POWER SEQUENCING

Some LCD flat-panel displays require power sequencing to prevent damage. For example, some panels can be damaged if the Vee bias supply is applied to the panel without first powering the control and data lines. The flat-panel video controller provides control signals for sequencing the power in the proper order to protect the panel from these effects. (The video BIOS controls the sequence and timing of these signals.) The SystemCard supports automatic sequencing of Vdd (+5V), Vee (bias voltages typically in the range of -30V<Vee<+30V), and +12V (for an external backlight power inverter). Use the ENAVDD and ENAVEE signals to switch the Vdd and Vee voltages respectively. Use ENABKL to control power to a backlight.

Ethernet Controller

This section describes how to configure and connect the Ethernet LAN interface.

On the **386X**, the Ethernet controller has its own setup utility, AMINSTAL.BAT. It allows you to configure the I/O locations, DMA channel, and Interrupt.

On the **486X**, the setup utility for the Ethernet controller is RSET8019.EXE.

There are no jumpers to set on the Ethernet interface, and no hardware configuration, other than connecting the network cable to an appropriate connector.

In addition, software configuration of the Ethernet interface requires that you install compatible networking software:

- Install the proper driver for the network operating system you will be running.
- Use the network operating system (NOS) client install procedure provided by your NOS software vendor and follow their instructions. The Ethernet controller on the SystemCard 386SX is NE2100-compliant and on the 486SX is NE2000-compliant.

CONNECTING TO THE ETHERNET CABLE

The Ethernet interface supports two Ethernet media, 10BaseT (twisted pair) and the AUI interface. The interface connectors are described in this section.

TWISTED PAIR INTERFACE

The twisted pair interface (10BaseT) appears on connector J15. J15 is an RJ45 modular connector. The following table lists the signals and pin numbers of J15:

J15 Pin	Function
1	+ Transmit Data
2	- Transmit Data
3	+ Receive Data
4	N/C
5	N/C
6	- Receive Data
7	N/C
8	N/C

Table 20. RJ45 Connector, J15

AUI INTERFACE

If you want to connect to a LAN using other than the twisted-pair interface, you can connect through the Adapter Unit Interface (AUI). The AUI connects to an external transceiver or MAU which, in turn, connects to your LAN cable. The AUI/MAU combination enables you to connect to fiber optic, thick net cable, or other Ethernet media.

Connect to the AUI interface at J16 using a 16-wire ribbon cable. Length of this cable should be less than 24 inches.

If you use the AUI interface, you must supply +12V. Connect the +12V to the power connector, J12. The +12V is supplied through a 1A fuse, F1.

Note: You cannot use the RJ45 interface and the AUI interface simultaneously.

Table 21 lists the signals and pin numbers of J16 and the wiring for a MAU-compatible DB-15:

J16 Pin	DB-15 Pin	Signal
1	4, 6, 11	Ground
2	9	- Collision Detect
3	2	+ Collision Detect
4	10	- Transmit Data
5	3	+ Transmit Data
8	12	- Receive Data
9	5	+ Receive Data
10	13	+12V Power*
6, 7,11, 12, 15	4, 11, 6	Signal Ground
16		Ground
13, 14	1, 7, 8, 14, 15	N/C
* +12 Volts is fused with a 1A fuse, F1		

Table 21. AUI Connector, J16

CompactFlash Removable Solid-State Disk

A connector is provided for a CompactFlash (CF) card. Connected to the IDE bus, the CF cards can provide from 2M to 60M bytes or more of removable solid-state disk storage. Documentation for the interface is provided by SanDisk and is included with the ZF System Card 386X Development Kit.

If you use the CF drive, it takes the place of an IDE hard disk drive in your system. Use Setup to configure your system for the IDE drives you use. Details about how to use Setup are provided in the *OEMmodule Data Book*.

The CF drive can be either an IDE master or slave. To boot from the CF drive, it must be formatted as a bootable drive and configured as master. To allow the system to boot from an IDE disk drive, the CF drive must be configured as slave. Install a jumper on JP7-1/2 to select the CF drive as master or JP7-2/3 to select the CF drive as slave.

Memory Expansion Sockets

The board has two 32-pin byte-wide sockets (**386SX**) or one 32-pin byte-wide memory chip socket(**486SX**) that can be used for additional storage. You can install any of a variety of 28-pin or 32-pin JEDEC-compliant memory devices, Flash, EPROM, NOVRAM (non-volatile static RAM with an internal backup battery), and Disk-On-Chip. If you use a Disk-On-Chip device, the sockets can emulate an additional disk drive.

> **Note**: If you install a 28-pin device in a socket, install pin 1 of the device in pin 3 of the socket. Leave pins 1, 2, 31, and 32 empty.

CONFIGURING THE MEMORY EXPANSION SOCKET

386SX SOCKET 1 (U15)

This socket is configured for a 32KB video BIOS EPROM starting at memory address C000h.

386SX SOCKET 2 (U16)

Socket is configured for a 64KB device, either DISC ON CHIP or EPROM, starting at memory address C800h.

486SX SOCKET 1 (U15)

Configure Socket 1 (U15) using the Custom Setup Screen in the CMOS Setup. . The Custom Setup Screen allows you to configure the device, size and memory starting address.

Digital I/O Interface

The SystemCard provides a built-in 12-bit digital I/O port that can be used to control or sense devices in your embedded system. For example, you can use the output bits to control indicator lamps, motors, solenoids, or other mechanical devices (with suitable buffering devices). TTL-level input bits can be used to sense the state of switches or optical interrupters. Using the digital I/O lines in combination, you can scan a keyboard (up to an 8 x 4 matrix).

The port is divided into two segments. The first segment is 8 bits (DIG0 - DIG7). You can use these signals for TTL input or TTL output. The port's direction is controlled by a bit in a control port. The second segment is 4 bits (DIG8 - DIG11), and can also be used for TTL input or TTL output.

The ports are non-inverting. That is, a "1" written to a port results in a TTL HIGH at the connector. Similarly, a TTL HIGH is sensed as a "1" upon input.

All digital I/O signals are current limited with a series 510 ohm resistor, and pulled up with a 10K ohm pull-up as shown in the following figure.

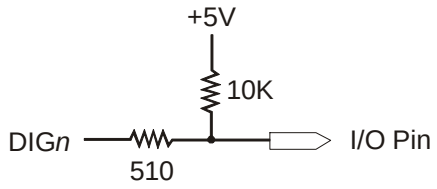

Figure 3. Digital I/O Signal Circuit

Table 22 lists the electrical specifications of the I/O signals.

Sym	Parameter	Test Conditions	Min	Max	Units
V_{OH}	Output High Voltage	I_{OH}=-4.0mA V_{CC}=Min	2.4		V
V_{OL}	Output Low Voltage	I_{OH}=-3.2mA V_{CC}=Min	2.4		V
V_{IL}	Input Low Voltage		0	0.80	V
V_{IH}	Input High Voltage		2.0	V_{CC}+0.5	V

Table 22. Digital I/O Signal Specifications

The 510 series resistors protect the I/O lines from current surges. In addition, they make it possible to directly drive LED lamps without requiring external components. Connect the LED anode to +5 volts and the LED cathode to the digital I/O signal to create an indicator lamp.

The digital I/O signals' input current is small. There is no significant voltage drop across the 510 ohm resistor when an input is driven with a TTL gate.

The 10K ohm pull-up resistors on input lines cause open inputs to read as a logic HIGH. This makes it possible to easily sense the state of switches without requiring external components. Connect one side of the switch to ground, the other to the digital input pin.

I/O pins are driven by the SystemCard using standard 8 MHz ISA I/O timing.

DIGITAL I/O CONNECTOR

Digital I/O signals appear on connector J23, a 16-pin dual-row ribbon cable connector. Table 23 shows the pinout of this connector.

J23 Pin	Function	J23 Pin	Function
1	Ground	9	DIG6
2	Ground	10	DIG7
3	DIG0	11	DIG8
4	DIG1	12	DIG9
5	DIG2	13	DIG10
6	DIG3	14	DIG11
7	DIG4	15	Ground
8	DIG5	16	Ground

Table 23. Digital I/O Connector, J23

SOFTWARE CONTROL OF THE I/O PORTS

386SX

DIGI IO 0:7 are set to inputs and DIGI IO 8:11 are set to outputs at the factory.

486SX

DIGI IO 0:11 are programmable as either inputs or outputs by writing to registers 1-3 of U20.

There are three actions for controlling the digital I/O ports: **Set Direction**, **Read Port**, and **Write Port**. The assembly code shown below illustrates how to control the digital I/O ports.

Set Direction

Use the following routine to change either port's direction to output or input. The power-up default state for both ports is "input."

Note: When a digital I/O port is set to output mode, it can still be read to determine its current state.

```
;-----------------------------------------
; Set an I/O port to output or input mode
;-----------------------------------------
INDEX      EQU     210h     ;write-only index port
DATA       EQU     211h     ;read/write data port
REG0       EQU     00       ;"Parking register"
REG3       EQU     03       ;digital i/o control register

Mov al,REG3           ;select register 3
Out INDEX,al

In al,DATA            ;read current state

;manipulate desired bits using And and Or assembly instructions
; DIG0-DIG7           Bit 0, 0=input, 1=output
; DIG8-DIG11          Bit 1, 0=input, 1=output

Out DATA,al

Move al,REG0          ;select parking register 0 to prevent accidental
Out INDEX,al          ;corruption of other registers
```

Read Port

The following assembly code illustrates how to read from an I/O port.

The DIG0 - DIG7 bits are controlled by Register 1 and the DIG8 - DIG11 bits are controlled by Register 2

```
;-----------------------------------------
; Read a byte from an I/O port
; (Assumes the port is set to input mode)
;-----------------------------------------
INDEX     EQU       210h
DATA      EQU       211h

Mov al,reg          ;select register 1 (01) for DIG0-DIG7 or
Out INDEX,al        ;register 2 (02) for DIG8-DIG11

In al,DATA          ;read data from port

;move the data wherever you want to store it
;    Data Bit    7     6     5     4     3     2     1     0
; Register 01   DIG7  DIG6  DIG5  DIG4  DIG3  DIG2  DIG1  DIG0
; Register 02    x     x     x     x    DIG11 DIG10 DIG9  DIG8

Move al,REG0        ;select parking register 0 to prevent accidental
Out INDEX,al        ;corruption of other registers
```


Write Port

The following assembly code illustrates how to write a data pattern to an I/O port.

The DIG0 - DIG7 bits are controlled by Register 1 and the DIG8 - DIG11 bits are controlled by Register 2

```
;-----------------------------------------
; Write bits to an I/O port
; (Assumes the port is set to output mode)
;-----------------------------------------
INDEX     EQU       210h
DATA      EQU       211h

Mov al,reg          ;select register 1 (01) for DIG0-DIG7 or
Out INDEX,al        ;register 2 (02) for DIG8-DIG11

Mov al,value        ;value is a binary data byte:
;    Data Bit    7     6     5     4     3     2     1     0
; Register 01   DIG7  DIG6  DIG5  DIG4  DIG3  DIG2  DIG1  DIG0
; Register 02    x     x     x     x    DIG11 DIG10 DIG9  DIG8

Out DATA,al         ;write data to port

Move al,REG0        ;select parking register 0 to prevent accidental
Out INDEX,al        ;corruption of other registers
```

Watchdog Timer

A watchdog timer is a circuit designed to either reset, cause an interrupt, or initiate some other recovery action if your program or hardware does not indicate that it is running properly. It usually is implemented for processes or activities that have some time predictability, such as the length of time it takes to perform a particular software function or complete the movement (or other change) of some physical system.

A typical application, for example, would initialize the watchdog timer when certain software functions start and end, or when a limit switch or optical interrupter connected to one of the digital I/O pins changes state. If the software crashes or gets stuck in a loop, or if the mechanical switch is not closed, the watchdog timer times out, causing a system reset.

The SystemCard has a built-in circuit that can generate a timeout after 1.6 seconds unless reset by its input signal, WDI. WDI is an internally-generated logic signal controlled by a BIOS call. As long as the timer is reset every 1.6 seconds or less, its output signal, WDO remains in its inactive state. Should the timer time out, the WDO signal goes high, triggering a reset.

The watchdog timer is disabled on Power-up. To enable the watchdog timer, set bit 0 of Register 9 of U20, a field programmable device.

PC/104 Expansion Bus Interface

Table 24 through Table 27 document the PC/104 expansion bus provided on the SystemCard. It also includes the pin designations for the standard ISA expansion bus interface signals for reference to standard PC bus expansion cards.

PC/104 P1A	ISA	Signal Name	Function	In/out
A1	A1	IOCHCK-	Bus NMI input	In
A2	A2	SD7	System Data bit 7	I/O
A3	A3	SD6	System Data bit 6	I/O
A4	A4	SD5	System Data bit 5	I/O
A5	A5	SD4	System Data bit 4	I/O
A6	A6	SD3	System Data bit 3	I/O
A7	A7	SD2	System Data bit 2	I/O
A8	A8	SD1	System Data bit 1	I/O
A9	A9	SD0	System Data bit 0	I/O
A10	A10	IOCHRDY	Processor Ready Ctrl	In
A11	A11	AEN	Address Enable	I/O
A12	A12	SA19	Address bit 19	I/O
A13	A13	SA18	Address bit 18	I/O
A14	A14	SA17	Address bit 17	I/O
A15	A15	SA16	Address bit 16	I/O
A16	A16	SA15	Address bit 15	I/O
A17	A17	SA14	Address bit 14	I/O
A18	A18	SA13	Address bit 13	I/O
A19	A19	SA12	Address bit 12	I/O
A20	A20	SA11	Address bit 11	I/O
A21	A21	SA10	Address bit 10	I/O
A22	A22	SA9	Address bit 9	I/O
A23	A23	SA8	Address bit 8	I/O
A24	A24	SA7	Address bit 7	I/O
A25	A25	SA6	Address bit 6	I/O
A26	A26	SA5	Address bit 5	I/O
A27	A27	SA4	Address bit 4	I/O
A28	A28	SA3	Address bit 3	I/O
A29	A29	SA2	Address bit 2	I/O
A30	A30	SA1	Address bit 1	I/O
A31	A31	SA0	Address bit 0	I/O
A32		GND	Ground	N/A

Table 24. PC/104 Expansion Bus Connector, A1 – A32

PC/104 P1B	ISA	Signal Name	Function	In/out
B1	B1	GND	Ground	N/A
B2	B2	RESETDRV	System reset signal	Out
B3	B3	+5V	+5 volt power	N/A
B4	B4	IRQ9	Interrupt request 9	In
B5	B5	-5V		N/A
B6	B6	DRQ2	DMA request 2	In
B7	B7	-12V		N/A
B8	B8	ENDXFR- (0WS-)	End Transfer (Zero wait state)	In
B9	B9	+12V		N/A
B10	B10			
B11	B11	SMEMW-	Mem Write (lower 1MB)	I/O
B12	B12	SMEMR-	Mem Read (lower 1MB)	I/O
B13	B13	IOW-	I/O Write	I/O
B14	B14	IOR-	I/O Read	I/O
B15	B15	DACK3-	DMA Acknowledge 3	Out
B16	B16	DRQ3	DMA Request 3	In
B17	B17	DACK1-	DMA Acknowledge 1	Out
B18	B18	DRQ1	DMA Request 1	In
B19	B19	REFRESH-	Memory Refresh	I/O
B20	B20	SYSCLK	System clock (8 MHz)	Out
B21	B21	IRQ7	Interrupt Request 7	In
B22	B22	IRQ6	Interrupt Request 6	In
B23	B23	IRQ5	Interrupt Request 5	In
B24	B24	IRQ4	Interrupt Request 4	In
B25	B25	IRQ3	Interrupt Request 3	In
B26	B26	DACK2-	DMA Acknowledge 2	Out
B27	B27	TC	DMA Terminal Count	Out
B28	B28	BALE	Address latch enable	Out
B29	B29	+5V	+5 volt power	N/A
B30	B30	OSC	14.318 MHz clock	Out
B31	B31	GND	Ground	N/A
B32		GND	Ground	N/A

Table 25. PC/104 Expansion Bus Connector, B1 – B32

PC/104 P2C	ISA	Signal name	Function	In/out
C0		GND	Ground	N/A
C1	C1	SBHE-	Bus High Enable	I/O
C2	C2	LA23	Address bit 23	I/O
C3	C3	LA22	Address bit 22	I/O
C4	C4	LA21	Address bit 21	I/O
C5	C5	LA20	Address bit 20	I/O
C6	C6	LA19	Address bit 19	I/O
C7	C7	LA18	Address bit 18	I/O
C8	C8	LA17	Address bit 17	I/O
C9	C9	MEMR-	Memory Read	I/O
C10	C10	MEMW-	Memory Write	I/O
C11	C11	SD8	System Data bit 8	I/O
C12	C12	SD9	System Data bit 9	I/O
C13	C13	SD10	System Data bit 10	I/O
C14	C14	SD11	System Data bit 11	I/O
C15	C15	SD12	System Data bit 12	I/O
C16	C16	SD13	System Data bit 13	I/O
C17	C17	SD14	System Data bit 14	I/O
C18	C18	SD15	System Data bit 15	I/O
C19		GND	Ground	N/A

Table 26. PC/104 Expansion Bus Connector, C0 – C19

PC/104 P2D	ISA	Signal Name	Function	In/out
D0		GND	Ground	N/A
D1	D1	MEMCS16-	16-bit memory access	In
D2	D2	IOCS16-	16-bit I/O access	In
D3	D3	IRQ10	Interrupt Request 10	In
D4	D4	IRQ11	Interrupt Request 11	In
D5	D5	IRQ12	Interrupt Request 12	In
D6	D6	IRQ15	Interrupt Request 15	In
D7	D7	IRQ14	Interrupt Request 14	In
D8	D8	DACK0-	DMA Acknowledge 0	Out
D9	D9	DRQ0	DMA Request 0	In
D10	D10	DACK5-	DMA Acknowledge 5	Out
D11	D11	DRQ5	DMA Request 5	In
D12	D12	DACK6-	DMA Acknowledge 6	Out
D13	D13	DRQ6	DMA Request 6	In
D14	D14	DACK7-	DMA Acknowledge 7	Out
D15	D15	DRQ7	DMA Request 7	In
D16	D16	+5V	+5 volt power	N/A
D17	D17	MASTER-	Bus master assert	In
D18	D18	GND	Ground	N/A
D19		GND	Ground	N/A

Table 27. PC/104 Expansion Bus Connector, D0 – D19

BIOS Setup

The SystemCard system BIOS (Basic Input Output System) supports a standard Setup function to configure system parameters (as well as advanced methods specifically designed for embedded systems — refer to the OEMmodule Data Book for details). The BIOS uses the Setup parameters to establish default conditions during system initialization, both during the Power On Self Test (POST) phase, and during system boot.

Setup parameters are normally stored in the CMOS configuration memory, a portion of the real-time-clock circuit. In the OEMmodule, the configuration data is also stored in an internal Flash memory device. Therefore, if there is no clock battery present in the system, or if the battery fails, configuration data is not lost when power is turned off. The BIOS automatically loads configuration values from the Flash copy of the data.

Note: If you do not use a battery in your system, leave the battery input open.

USING SETUP

To enter the Setup function, press the <Del> key during POST. <Del> can be asserted at any time prior to boot.

Note: When you change Setup parameters, the new values do not take effect until the system is rebooted.

There are two Setup screens:

- **Main Menu Screen** — Displays a top-level menu of Setup choices
- **Basic CMOS Configuration** — Displays the standard CMOS options you can set for your system.

For details about how to set the various parameters using Setup, refer to the OEMmodule Data Book.

Embedded DOS-ROM

Each SystemCard has General Software's Embedded DOS-ROM (EDOS-ROM) installed in Flash memory internal to the OEMmodule. The system can be set up to boot directly from EDOS-ROM.

Specifications

ABSOLUTE MAXIMUM RATINGS*

Absolute Maximum Voltage on any pin, with respect to Ground .....-0.3V to +6.5V

Storage Temperature (case) .....-55°C to +80°C (-67°F to +176°F)

OPERATING CONDITIONS*

Supply Voltage (V_{CC}) .....4.75V to +5.25V

Case Temperature (under bias) ..... 0°C to 70°C (32°F to 158°F)

* Stresses above those listed above can cause permanent damage to the board. These values are stress ratings only and do not imply that the device should be operated at these extremes. Exposure beyond the "Operating Conditions" may affect device reliability. Note that some power supplies exhibit voltage spikes when AC power is switched on or off or when voltage transients appear on the AC power line. If this possibility exists it is suggested that you use a clamp circuit on the DC supply.

Literature References

The following references are for information about the PC architecture, the 386SX microprocessor, the PC DOS, and the PC BIOS.

ISA System Architecture

MindShare, Inc., Tom Shanley and Don Anderson
Internet: mindshar@interserv.com
CompuServe: 72507,1054
Published by Addison Wesley, Inc.

AT Bus Design

Edward Solari
Anabooks
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Personal Computer Bus Standard P996

Institute of Electrical and Electronic Engineers, Inc.
445 Hoes Lane
Piscataway, NJ 08854

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386 SX Microprocessor Programmer's Reference Manual
Intel
1751 Fox Drive
Suite 29000
San Jose, CA 95131

Technical data on Embedded DOS 6-XL

General Software, Incorporated
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The LIM 4.0 Expanded Memory Specification:

Lotus/Intel/Microsoft Expanded Memory Specification, Version 4.0
Lotus Development Corporation
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